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Exhibit B

FEATURING

A Device that Has Traveled in Outer Space

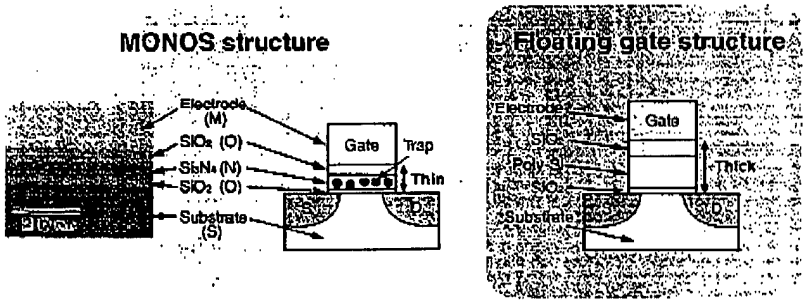
Low-Cost Embedded Nonvolatile Memory Device Technology: MONOS

- **High reliability**
  – Charge storage in a nitride film –
- **Narrow distribution of threshold voltages obviates the need for a "verify" operation to match distribution widths narrowly**
  – Makes circuit design easier –
- **Simple device structure makes chips easier to manufacture**
  – Expected to be usable through the 0.1 μm generation –
- **Low-cost embedded nonvolatile memory technology**
  – Low-voltage write and erase operations achieved by the use of hot carrier injection–

While MONOS (metal-oxide-nitride-oxide-semiconductor) is not a new nonvolatile memory technology, it has not received much attention until recently. The floating gate technology has remained as the mainstream nonvolatile memory technology, mostly due to the MONOS data retention characteristics being inferior. However, MONOS' reputation has begun to change over in recent years.

Figure 1 compares the MONOS and floating gate device structures. As can be seen in figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data. In the US, MONOS is used in satellites and spacecraft that wander for long periods between the planets. So why is it that MONOS, which is thought to have poor data retention characteristics, is used in the harsh environment of outer space, where they are constantly bombarded by high-energy particles? The reason lies in the structure and operating principles of the MONOS device. MONOS devices are actual highly stable and reliable devices.

Recently, the idea of storing 2 bits in a single memory transistor cell by using the features associated with storing charge on in the insulation layer in the MONOS device has been proposed. This makes it possible for MONOS to be the highest density nonvolatile memory technology, and has resulted in increasing interest in this technology. Another point is that the limits of the floating gate nonvolatile memory technology are now in sight, and MONOS is seen as having the potential to be the next generation nonvolatile memory technology. Sony's researchers already see how MONOS can be adapted for use through the 0.1 μm feature size generation. Furthermore, Sony is now developing MONOS as a key technology for product differentiation in Sony's system-on-chip (SoC) business.



■ Figure 1 MONOS and Floating Gate Structures Comparison

MONOS Device Structure and Operating Principles

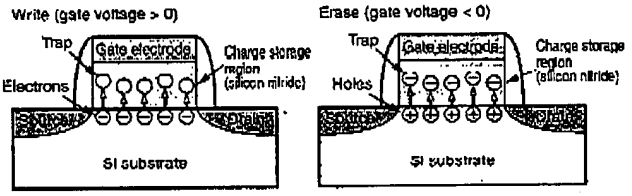
As shown in figure 1, the MONOS structure consists of ONO film layers (oxide-nitride-oxide) between the substrate and the gate. While the nitride film in the center of the ONO film layers is an insulator, there are large numbers of traps located in that layer and it can capture and store charge. This layer can be made to function as a charge storing means by injecting and rejecting charge from these traps.

There are two techniques for injecting and rejecting charge. One is a write and erase method in which electrons are injected or rejected with tunnel current technique over the whole area under the gate electrode as shown in figure 2. The other method uses hot carriers as shown in figure 3. The tunnel current technique achieves a larger number of write/erase cycles and assures high reliability. In contrast, the hot carrier method allows lower write and erase operating voltages to be used and achieves higher speeds. Lowering the operating voltage also leads to reduced manufacturing costs, and is effective for one-time programming (OTP) and multi-time programming (MTP) products. Recently, the idea of MONOS devices that store 2 bits in a single memory transistor cell using this principle has proposed. These are called NROM devices.

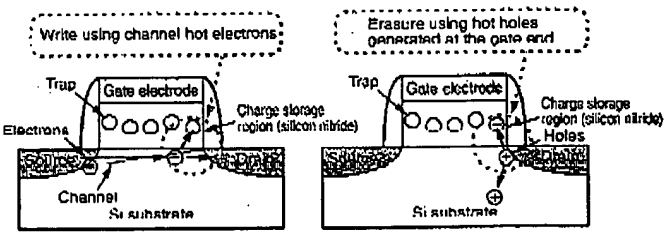
High Reliability

MONOS' main advantage lies in its stability and durability. As shown in figure 4, there is almost little charge leakage in MONOS devices even if there are defects in the extremely thin oxide film between the nitride layer that stores the charge and the substrate. This is because charge is stored in an insulating film layer. In contrast, in the floating gate type device, all stored charge is lost if a defect is created at even one location. This is like the shipbuilding technique in which large numbers of isolated chambers are used. If a defect is opened in one, the area that is flooded is limited to that chamber. That is, even if a defect is created between the substrate and the layer (nitride film) that stores the charge, it is impossible for all the charge stored in the insulating film to escape through that defect. In contrast, conventional floating gate ships (devices) would flood and sink immediately if even one defect appeared. This is because the floating gate, which stores the charge, is itself a conductor. This MONOS durability is the reason MONOS is used in outer space, where devices are constantly bombarded by high-energy particles.

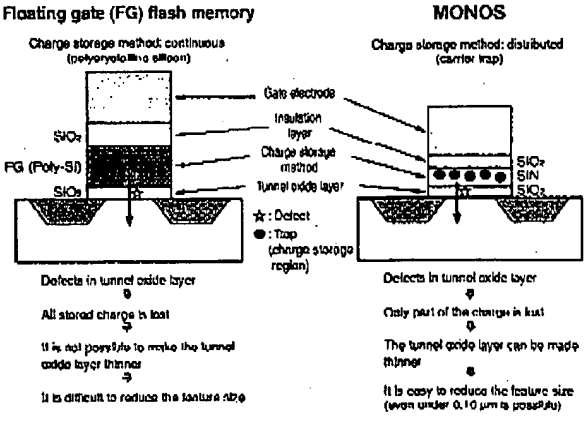
MONOS has another advantage. That advantage is that it leaks. It cannot be denied that this is the reason that MONOS is not widely used. However, as our study of the MONOS structure has progressed, and we have had more experience using MONOS, we have come to realize the following. There is no sample-to-sample variation in the amount of leakage in MONOS devices. That is, all boats (devices) leak water at the same rate. This means that it is possible to predict when to get off the boat in safety. That is, these boats are actually much safer than boats that appear solid but may actually rupture and sink at any time.



■ Figure 2 MONOS Write and Erase Operations Using F-N Tunnel Current Injection Technique Conceptual Overview



■ Figure 3 MONOS Write and Erase Operations Using Hot Carriers Injection Technique Conceptual Overview



■ Figure 4 MONOS Features: Charge Does not Escape even with Defects in the Oxide Layer

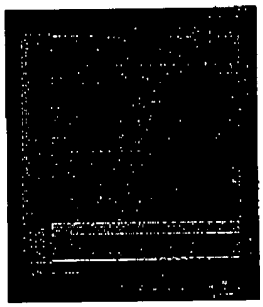
FEATURING

Narrow Threshold Voltage Distribution Obviates the Need for Operations to Narrow the Distribution

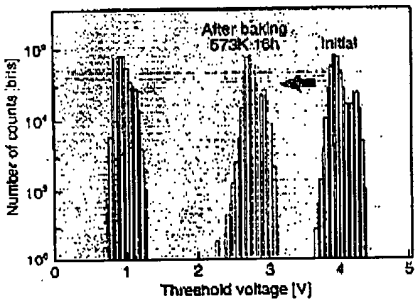
Sony has taken the lead in this area by creating the 4 Mbit MONOS test memory chip shown in figure 5. (This device was announced at the 2001 IEDM conference.) Figure 6 shows the accelerated test results for the written threshold voltage distribution retention characteristics. Although the threshold voltage falls, the distribution does not break. Furthermore, as shown in table 1, the width of the distribution itself is narrower, being only 1/3 that of the conventional floating gate device, and thus is extremely well matched. Also, the threshold voltage distribution does not break after repeated write and erase cycles. Figure 7(a) shows the change in the width of the distribution with writing, and figure 7(b) shows that change with erasure. As you can see, the width of the distribution does not change with these processes. Even with repeated write and erase cycles, the distribution remains narrow. (See figure 8.) This is one of MONOS' superior characteristics, and is a significant advantage when designing memory circuits. In the conventional floating gate device, the threshold voltage distribution must be narrowed with an operation called "verify" during write and erase. This is a difficult circuit operation and complicates circuit design. The MONOS structure may be able to obviate the need for this "verify" operation.

Device with a Simple Ease to Fabricate Structure

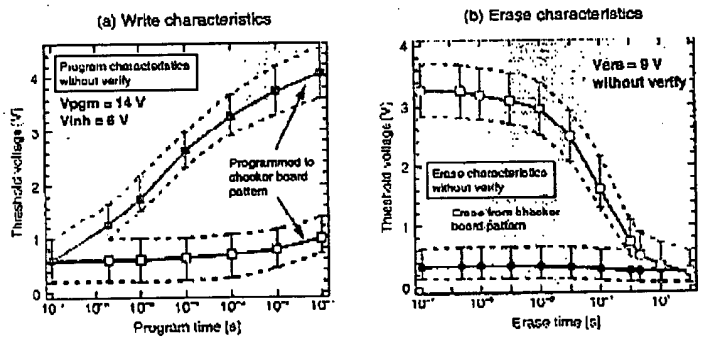
Another significant feature of the MONOS structure is the simplicity of that structure. Figure 9 shows the cross section of a MONOS device imaged with a transmission electron microscope (TEM). At first look, it appears to be identical to an ordinary MOS transistor. Sony already sees the way to use this structure in 0.1 µm generation devices. The simplicity of this structure is also extremely important for embedding these devices in larger chips. This is because the simpler the structure the fewer the additional fabrication steps required for embedding. If only MONOS transistors are added, only 2 or 3 mask steps need to be added. Normally, embedding other types of flash memory requires an additional 6 or 7 masks. This is because these other devices require that the high-voltage transistors that handle the high voltages required for write and erase operations must be created separately.



■ Figure 5 4 Mbit MONOS Test Chip



■ Figure 6 4 Mbit MONOS Test Chip Memory Retention Characteristics



■ Figure 7 Write and Erase Characteristics of MONOS Threshold Voltage Distribution

■ Table 1 MONOS and Floating Gate Threshold Voltage Distributions Comparison

	MONOS	Floating gate devices	
	Chip product	ref.1	ref.2 ref.3
Write state	0.057	0.1	0.165
Erase state	0.058	0.15	0.15

Standard deviation (V)

Standard deviation in MONOS is about 1/3

[1] K.Yoshikawa, et al., IEDM92, p.595 (1992).
[2] R.Shirota, NVSMW 2000, p.22 (2000).
[3] P.L.Rolandi, et al., NVSMW 2000, p.75 (2000).

Low-Cost Embedded Nonvolatile Memory Technology

If nonvolatile memory could be embedded with only the addition of 2 or 3 masks, that is, with only a cost increase of about 10% over that of the original chip, we could expect a large demand for OTP and MTP applications. Another way of looking at this would be that low-cost embedded nonvolatile memory technology would function as a product differentiation technology. Specific examples that would be possible include inclusion of embedded nonvolatile memory in the camera processor IC that forms, along with the CMOS image sensor, a camera module, in a GPS module that fits in a Memory Stick slot, or in a camera module interface chip. (See figure 10.)

Other applications where this would be useful include the programmable impedance matching circuit used in high-precision D/A converters and high-precision power supplies and the recording of data used for chip authentication.

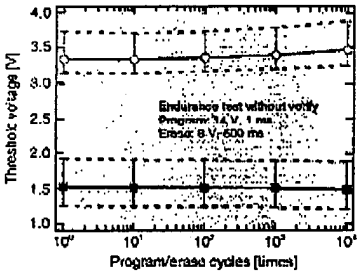
Sony is now studying the possibility of reducing the MONOS write and erase voltages to realize low-cost embedded nonvolatile memory technology using only 2 or 3 additional masks. Sony is attempting to reduce the voltages required by switching from the use of F-N tunnel current, which requires 12 to 14 V for write and erase, to a technique that uses hot carriers. Figure 11(a) shows the write characteristics when channel hot electrons are used, and figure 11(b) shows the erase characteristics using hot hole injection. With absolute voltages around 5 to 6 V, these techniques can achieve fully adequate write and erase operations.

Future Developments

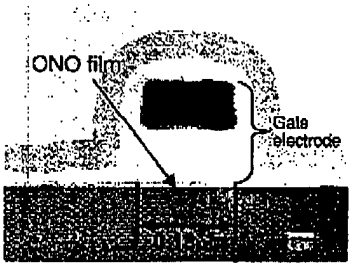
Sony is making progress on embedding MONOS nonvolatile memory in a 0.18 μm CMOS process. We are working on creating new applications and expect to release products using this technology during 2003.

This one process is not the only process that requires embedded nonvolatile memory. To take maximum advantage of this newly-developed technology, Sony plans to apply it in as many processes as possible. We think that MONOS' stability and durability will make this easy.

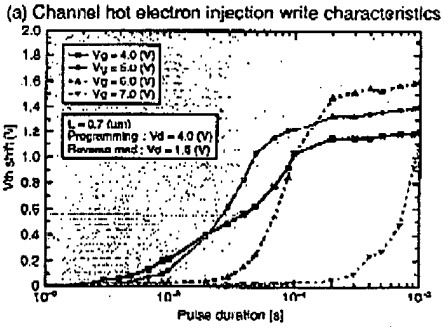
Keep your eye on Sony's low-cost nonvolatile memory technology.

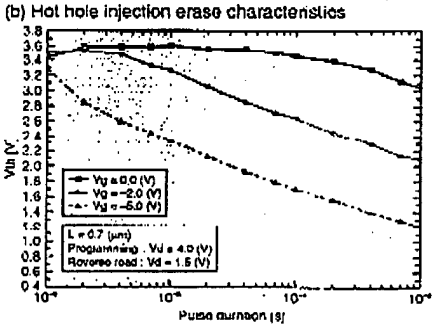


■ Figure 8 4 Mbit MONOS Test Chip Endurance Characteristics

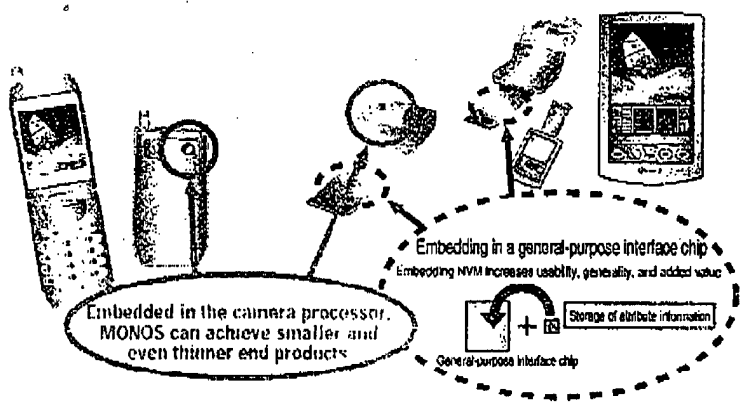


■ Figure 9 TEM Photograph for MONOS Memory Transistor





■ Figure 11 Characteristics of the Embedded Low-Voltage MONOS Memory Cell



■ Figure 10 Embedded MONOS Applications